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10/754,726	01/12/2004	Chao-Hsin Lu	LUCH3011/EM	1341

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/754,726	LU, CHAO-HSIN
	Examiner	Art Unit
	Long Nguyen	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 13-23* is/are rejected.

7)☒ Claim(s) *6-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on 4/27/05 has been received and entered in the case.

2. The objection to the specification in the last office action has been overcome based on applicant's persuasive argument.

Claim Objections

3. Claims 19-23 are objected to because of the following informalities:

In claim 19, lines 3, 5, 7 and 9, "or" should be changed to --and-- since the phrase "one of" is recited.

Claims 20-23 are objected to because they include the informalities of claim 19.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 14-17 and 19-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 14, the phrase "the third transistor and the fourth transistor are directly coupled to ground or both" on lines 4-5 is indefinite because it is not clear what applicant means by "or both" in the above phrase. Clarification and/or appropriate correction is required.

Claims 15-17 are indefinite because they include the indefiniteness of claim 14.

With respect to claim 19, the phrase "the third transistor and the fourth transistor are directly coupled to ground or both" on the last 2 lines of the claim is indefinite because it is not clear what applicant means by "or both" in the above phrase. Clarification and/or appropriate correction is required.

Also in claim 19, the recitation "between the third transistor and the ground" on line 8 is indefinite because it is misdescriptive since it is clearly from the drawings that the fourth transistor is coupled between the second transistor and ground (i.e., the fourth transistor does not coupled between the third transistor and ground as recited on line 8). Clarification and/or appropriate correction is required.

Claims 20-23 are indefinite because they include the indefiniteness of claim 19.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-5, 13 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Lye (USP 6,566,933).

With respect to claim 1, Figure 3 of the Lye reference discloses a driving apparatus, which includes: an output circuit (70, 72) to output a differential signal (the output signals of M1-M4); a switch circuit (S5-S12) coupled to the output circuit for controlling a phase of the differential signal (controlling the on/off of M1-M4, so the phase of the differential output signal

is controlled by the switched circuit); and a reference current control circuit (I2, I1, whichever circuit that provides VDD, and whichever circuit/terminal that provides reference VSS) to provide a control voltage (VDD – voltage drop across I2, i.e., the voltage at the junction connections of M3-M4 and I2, and voltage across I1, i.e., the voltage at the junction connection of M1-M2 and I1) to the output circuit such that the magnitude of the differential signal is determined based on the control voltage (i.e., the magnitude of the differential output signal is depended on the voltage at the junction connections of M3-M4 and I2, and the voltage at the junction connection of M1-M2 and I1).

With respect to claim 2, Figure 3 shows the output circuit (70, 72) includes a first transistor (M3), a second transistor (M4), a third transistor (M1) and a fourth transistor (M2), operational voltage source (source that provide Vdd), and ground (Vss terminal).

With respect to claim 3, Figure 3 shows the first and second transistors (M3, M4) are PMOS transistors, and the third and fourth transistors (M1, M2) are NMOS transistors.

With respect to claim 4, it is seen in the operation of Figure 3 that the control voltage includes a first control voltage (the voltage at the junction connections of M3-M4 and I2) for controlling currents of the first and second transistors (M3 and M4, i.e., the drain-source current of M3 and M4 also depending on the voltage at the junction node of M3-M4 and I2), and a second control voltage (the voltage at the junction connection of M1-M2 and I1) for controlling currents of the third and fourth transistors (M1 and M2, i.e., the drain-source current of M1 and M2 also depending on the voltage at the junction node of M1-M2 and I1).

With respect to claim 5, it is seen in the operation of Figure 3 that the switch circuit (S5-S12) is for selectively turning OFF either the first (M3) and fourth (M2) transistors or the second

(M4) and the third (M1) transistors (i.e., when D closed switches S5, S8, S9 and S12, then D/ opened switches S6, S7, S10 and S11, so transistors M3 and M2 will be turning ON while transistors M4 and M1 will be turning OFF; and vice versa transistors M4 and M1 will be turning ON while transistors M3 and M2 will be turning OFF).

With respect to claim 13, because the driving apparatus in Figure 3 is a differential signal driving apparatus with low (minimize) power dissipation, so it meets the limitation that the driving apparatus is a LVDS driving apparatus.

With respect to claim 18, Figure 3 of Lye shows the reference current control circuit (I2, I1, whichever circuit that provides VDD, and whichever circuit/terminal that provides reference VSS) comprises a current source (I2, I1) for generating a reference current (I2, I1), wherein the control voltage (the voltage at the junction connections of M3-M4 and I2, and the voltage at the junction connection of M1-M2 and I1) corresponding to the reference current (I2, I1, respectively due to Ohm's law V = IR).

8. Claims 14-22 are rejected under 35 U.S.C. 102(e) as being anticipated by anticipated Cook et al. (USP 6,788,116).

With respect to claim 14, Figure 1 of the Cook et al. reference discloses a driving apparatus, which includes: an output circuit (first to fourth transistors M1-M4) to output a differential signal (Vouta, Voutb); a switch circuit (whichever circuit that is used to generated signals Vina and Vinb to perform switching of the transistors M1-M4 is reasonable to be considered as the switch circuit) coupled to the output circuit for controlling a phase of the differential signal (controlling the on/off of M1-M4, so the phase of the differential output signal is controlled by the switched circuit); and a reference current control circuit (M0 with 22, and the

circuit/terminal that is used to provide reference VSS/GND) to provide a control voltage (VDD – voltage drop across M0, i.e., the voltage at the junction connection of M1-M2 and M0, and the ground voltage) to the output circuit such that the magnitude of the differential signal is determined based on the control voltage (i.e., the magnitude of the differential output signal is depended on the voltage at the junction connection of transistors M1-M2 and M0). Note that third and fourth transistors (M3 and M4) are directly coupled to ground.

With respect to claim 15, Figure 1 shows the first and second transistors (M1, M2) are PMOS transistors, and the third and fourth transistors (M3, M4) are NMOS transistors.

With respect to claim 16, it is seen in the operation of Figure 1 that the control voltage includes a first control voltage (the voltage at the junction connections of M1-M2 and M0) for controlling currents of the first and second transistors (M1 and M2, i.e., the drain-source current of M1 and M2 also depending on the voltage at the junction node of M1-M2 and M0), and a second control voltage (the voltage at the reference VSS/GND) for controlling currents of the third and fourth transistors (M3 and M4, i.e., the drain-source current of M3 and M4 also depending on the voltage at the reference VSS/GND).

With respect to claim 17, it is seen in the operation of Figure 1 that the switch circuit is for selectively turning OFF either the first (M1) and fourth (M4) transistors or the second (M2) and the third (M3) transistors (Col. 3, lines 45-50).

With respect to claim 18, Figure 1 shows the reference current control circuit includes a current source (I0) for generating a reference current (Id), wherein the control voltage (the voltage at the junction connection of M1-M2 and M0) corresponding to the reference current (Id).

With respect to claims 19 and 22, Figure 1 of Cook et al. shows a circuit for outputting a differential signal (Vouta, Voutb), which includes: a first transistor (M1) coupled to an operational voltage source (Vdd) for receiving one of a first control signal (Vina) and a third control signal (signal at the junction node of transistors M1-M2 and M0); a second transistor (M2) coupled to the operational voltage source (Vdd) for receiving one of the first control signal (Vina) and the third control signal (signal at the junction node of transistors M1-M2 and M0); a third transistor (M3) coupled between the first transistor (M1) and ground (VSS/GND) for receiving one of a second control signal (Vinb) and a fourth control signal (signal at the VSS/GND terminal); and a fourth transistor (M4) coupled between the second transistor (M2) and ground (VSS/GND) for receiving one of the second control signal (Vinb) and the fourth control signal (signal at the VSS/GND terminal) . Note that third and fourth transistors (M3 and M4) are directly coupled to ground.

With respect to claim 20, it is seen in the operation of Figure 1 that while the first (M1) and fourth (M4) transistors generated current (i.e., M1 and M4 are ON), the second (M2) and the third (M3) transistors are OFF; and while the second (M2) and third (M3) transistors generated current (i.e., M2 and M3 are ON), the first (M1) and the fourth (M4) transistors are OFF (Col. 3, lines 45-50).

With respect to claim 21, it is seen in the operation of Figure 1 that the magnitude of the differential signal (Vouta, Voutb) is determined according to the first and second control signals (that is because the input signals Vina and Vinb turns on/off the transistors M1-M4 to provides Hi/Lo to the outputs Vouta and Voutb). Further, if reading from Figure 1 for the first signal (signal at the junction node of M1-M2 and M0), the second signal (signal at VSS/GND

terminal), the third signal (Vina), the fourth signals (Vinb), and the first to fourth transistors (M1-M4) then it is clearly that the magnitude of the differential signal (Vouta, Voutb) is determined according to the first and second control signals (signal at the junction node of M1-M2 and M0, and signal at the VSS/GND terminal).

9. Claims 19-21 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by anticipated Hass (USP 6,720,805).

With respect to claims 19-21 and 23, Figure 1A of the Hass reference shows a circuit for generating a differential output signal (OUTP, OUTN), which includes: a first transistor (M1) coupled to an operational voltage source (Vdd) for receiving one of a first control signal and a third control signal (A, AN); a second transistor (M2) coupled to the operational voltage source (Vdd) for receiving one of the first control signal and the third control signal (A, AN); a third transistor (M3) coupled between the first transistor (M1) and ground (VSS) for receiving one of a second control signal and a fourth control signal (BN, B); and a fourth transistor (M4) coupled between the second transistor (M2) and ground (VSS) for receiving one of the second control signal and the fourth control signal (BN, B) . Note that first and second transistors (M1, M2) are directly coupled to the operational voltage source (Vdd); and from the operation of Figure 1A, it is seen that while the first (M1) and fourth (M4) transistors generated current (i.e., M1 and M4 are ON), the second (M2) and the third (M3) transistors are OFF, and while the second (M2) and third (M3) transistors generated current (i.e., M2 and M3 are ON), the first (M1) and the fourth (M4) transistors are OFF (when A is Hi, then B is also Hi so M1 and M4 are ON to generate current, while AN and B are Lo so M2 and M3 are off, and similarly, when A is Lo, then B is also Lo so M1 and M4 are OFF, while AN and B are Hi so M2 and M3 are ON). Figure 1A also

shows that the signals (A, AN, B, BN) are provided by a reference current control circuit (XBIAS, XPDRV) which includes a current source (current through M8, or current through M11) for generating a reference current (current through M8, or current through M11), wherein the first and second control signals are corresponding to the reference current (the amplitudes of A, AN, B, and BN depending on the currents flowing through M11 and M8).

Allowable Subject Matter

10. Claims 6-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if rewritten to overcome the rejection under 35 U.S.C. 112, 2nd paragraph, set forth above.

Response to Arguments

11. Applicant's arguments filed on 4/27/05 have been fully considered but they are not persuasive.

With respect to claim 1, applicant argues that the circuit in Figure 3 of the Lye reference fails to teach or suggest that the currents I1 and I2 are determined by the VDD or GND or the voltage VMID, and that the outputs of differential pairs 70 and 72are determined based on the VDD or GND or the voltage VMID. However, this argument is not persuasive because the claim's limitations do not require that I1 and I2 are determined by the VDD, GND or VMID; and that the output of 72 and 70 clearly depends on VDD and GND because the amplitudes of the output signals of 72 and 70 depends on the power supply voltages to the circuit of 70 and 72 since the voltage at the junction node of transistors M3 and M4 depends on VDD and the voltage at the junction node at the junction node of transistors M1 and M2 depends on I1 and Vss.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

July 5, 2005

LONG NGUYEN
PRIMARY EXAMINER